REMARKS

Claims 1-21 are currently pending in the application. In view of the following remarks Applicants request reconsideration of the rejected claims, and allowance of the entire application.

Allowed Claims

Applicants appreciate the indication that claims 2, 3, 11-16, 20 and 21 contain allowable subject matter and would be allowable if rewritten to include all the features of the rejected base claim and intervening claims. Applicants, however, submit that all of the claims are in condition for allowance for the reasons set forth below.

35 U.S.C. §103 Rejection

Claims 1, 4-10 and 17-19 were rejected under 35 U.S.C. §103(a) for being unpatentable over non-patent documents Shobaki in view of Mosensoson. Applicants submit that the rejection of claims 1, 4-10 and 17-19 should be withdrawn in view of the following comments.

The invention is directed to an on-chip logic analyzer (OCLA) which allows for testing and debugging real-time system-on-chip (SOC) systems, e.g., digital signal processing chips, without interrupting operations of the signal processing unit. Traditional emulator schemes for debugging and testing real-time signal processors have relied on the ability to start and stop the processor by using a variety of mechanisms, which includes setting software breakpoints and single stepping through the machine code. A major drawback of the traditional emulation schemes is that the processor must be stopped once a breakpoint is reached or the instruction is executed. This imposes significant problems in real-time systems. But, in the presently claimed

invention, for example, a

> data capturing unit captures data processed by said signal processing unit in response to said control signals from said host unit and transfers said captured data to said host unit without interrupting operations of said signal processing unit.

In this manner, the invention provides a solution to the observability problems that have not been even recognized by conventional SOC system testing/debugging schemes.

As recited, the OCLA system of the invention includes an on-chip VHDL (hardware description language) macro embedded in an SOC device, a host system, and a user interface. The VHDL macro includes the data capturing logic which monitors the operations of other VHDL macro components, particularly the signal processing logic and data buses, and captures and transfers data to the host system for testing and debugging without interrupting the operation of the target system. This is possible, in part, because the data capturing logic is embedded within the VHDL macro with other VHDL macro components.

The data capturing unit includes control logic, communication logic and a trace buffer (which may be SRAM). The control logic coordinates all operations of the OCLA portion of the VHDL macro. Upon power-on, the OCLA system monitors the operations of the VHDL macro for trigger conditions. In examples, the control unit loads a trace word from the captured data and performs multiplexing operations by using a mask value and match value. The communication logic provides a communication interface between the data capturing unit and the host system; that is, the communication logic takes in the control signals from the host system card into the VHDL macro and transfers to the control logic, and transfers the data captured by the trace buffer to the host system. Relevant data for testing and debugging is thus captured without interrupting any internal operation of a VHDL macro because the data capturing logic is

embedded within the VHDL macro to observe or watch the internal operations of the VHDL macro. Thus, the invention enables non-obtrusive real-time data acquisition for SOC signal processing systems.

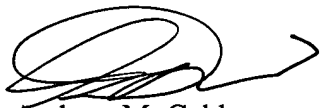
Shobaki shows a verification system but does not appear to show a single chip device internally including a signal processing unit, a plurality of memory blocks and a data capturing unit. As discussed above, the data capturing logic is embedded within the VHDL macro with other VHDL macro components. The Shobaki reference discloses a hardware based monitoring system (MAMon), which integrates small hardware components in the SOC and works like a probe by listening to logic or system level events in a passive manner. MAMon may also be activated by software which writes to a specific register. Detected events are time stamped and sent to a host based tool environment where the events are stored in a database. As disclosed at page 57, MAMon includes a probe unit (PU) which is integrated into the design HDL code, and connected to signals that constitute the events to be monitored. The PU performs detection, time stamping and recording of events. Also, as shown in Figure 3 of Shobaki, the PU includes an event detector. The condition expressions that define events are hard coded into the event detector. There does not appear to be a mask value and a match value, nor does there appear to be any discussion concerning a data control unit being embedded within a VHDL macro, for example amongst other features pointed out by the Examiner.

Mosensoson shows a SOC verification system. The SOC design is an implementation technology, where the SOC may contain, for example, a processor, processor bus, a peripheral bus and peripheral devices.

CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submit that all of the stated grounds for rejection have been overcome or rendered moot. Applicants submit that all of the claims are allowable and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Prompt and favorable consideration of this reply is respectfully requested.

Respectfully submitted,



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